

Powered-off Protection, 1 Ω, 1.8 V to 5.5 V, SPDT Analog Switch (2:1 Multiplexer)

DESCRIPTION

The DG2012E is a high performance single-pole, double-throw (SPDT) analog switch designed for 1.8 V to 5.5 V operation with a single power rail.

Fabricated with high density CMOS technology, the device achieves low on resistance of 1 Ω at a 5 V power supply, low power consumption, and fast switching speeds.

The DG2012E can handle both analog and digital signals and permits signals with amplitudes of up to V₊ to be transmitted in either direction. Its control logic inputs can go over V₊ up to 5.5 V. It features break before make switching performance. Its -3 dB bandwidth is typically 160 MHz.

A powered-off protection circuit is built into the switch to prevent an abnormal current flow from COM pin to V₊ during the power-down condition. Each output pin can withstand greater than 7 kV (human body model).

Operation temperature is specified from -40 °C to +85 °C. The DG2012E is available in SC-70-6L package.

FEATURES

- Low switch on-resistance (1 Ω)
- 1.65 V to 5.5 V single supply operation
- Isolation in powered-off mode
- Control logic inputs can go over V₊
- Low charge injection (5 pC)
- Low total harmonic distortion
- Break before make switching
- Latch-up performance exceeds 300 mA per JESD 78
- ESD tested
 - 7000 V human body model (JS-001)
 - 1000 V charge device model (JS-002)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



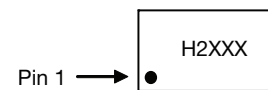
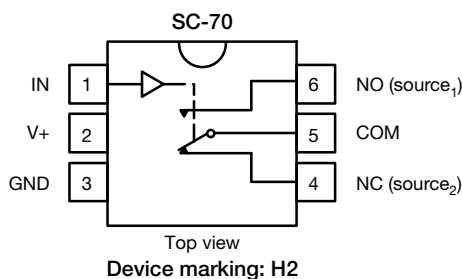
Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Smartphones and tablets
- Consumer and computing
- Portable instrumentation
- Medical equipment

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device marking: H2XXX
XXX = date / lot traceability code

TRUTH TABLE		
LOGIC	NC	NO
0	On	Off
1	Off	On

ORDERING INFORMATION		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	SC-70-6	DG2012EDL-T1-GE3



ABSOLUTE MAXIMUM RATINGS			
PARAMETER			UNIT
V+, COM, NC, NO, IN reference to GND			V
Continuous current (NO, NC, and COM pins)			mA
Peak current (pulsed at 1 ms, 10 % duty cycle)			
Storage temperature (D suffix)			°C
Power dissipation (packages) ^a	6-pin SO-70 ^b	250	mW
ESD / HBM	JS-001	7000	V
ESD / CDM	JS-002	1000	
Latch up	Per JESD78 with 1.5 x voltage clamp	300	mA

Notes

- a. All leads welded or soldered to PC board
- b. Derate 3.1 mW/°C above 70 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 5 V)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, ± 10 %, V _{IN} = 0.8 V or 2.4 V ^e	TEMP. ^a	LIMITS -40 °C to +85 °C			UNIT
				MIN. ^b	TYP. ^c	MAX. ^b	
Analog Switch							
Analog signal range ^d	V _{NO} , V _{NC} V _{COM}		Full	0	-	V+	V
On-resistance	R _{ON}	V+ = 4.5 V, V _{COM} = 0.5 V / 2.5 V, I _{NO} , I _{NC} = 10 mA	Room Full ^d	-	1	1.6 2	Ω
R _{ON} flatness ^d	R _{ON} flatness	V+ = 4.5 V, V _{COM} = 0 V to V+, I _{NO} , I _{NC} = 10 mA	Room	-	0.2	0.5	
R _{ON} match ^d	ΔR _{ON}		Room	-	-	0.3	
Switch off leakage current ^f	I _{NO(off)} I _{NC(off)}	V+ = 5 V V _{NO} , V _{NC} = 0.5 V / 4.5 V, V _{COM} = 4.5 V / 0.5 V	Room Full	-5 -20	-	5 20	nA
	I _{COM(off)}		Room Full ^d	-5 -20	-	5 20	
Channel-on leakage current ^f		I _{COM(on)}	Room Full ^d	-5 -20	-	5 20	
Power down leakage	I _{COM(PD)}	V+ = 0 V, V _{COM} = 4.5 V, V _{IN} = GND	Full ^d	-1	-	1	
Digital Control							
Input high voltage	V _{INH}		Full	2.4	-	-	V
Input low voltage	V _{INL}		Full	-	-	0.8	
Input capacitance ^d	C _{IN}		Full	-	3	-	pF
Input current ^f	I _{INL} or I _{INH}	V _{IN} = 0 V or V+	Full	-1	-	1	μA
Dynamic Characteristics							
Turn-on time ^d	t _{ON}	V _{NO} or V _{NC} = 3 V, R _L = 300 Ω, C _L = 35 pF	Room Full ^d	- -	15 -	32 35	ns
			Turn-off time ^d	t _{OFF}	Room Full ^d	- -	
Break-before-make time ^d	t _d				Room	1	
Charge injection ^d	Q _{INJ}		C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room	-	8	
Off-isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room	-	-63	-	dB
Crosstalk ^d	X _{TALK}		Room	-	-63	-	
N _O , N _C off capacitance ^d	C _{NO(off)} C _{NC(off)}	V _{IN} = 0 V or V+, f = 1 MHz	Room	-	16	-	pF
			Channel-on capacitance ^d	C _{ON}	Room	-	
Power Supply							
Power supply current	I+	V _{IN} = 0 V or V+	Full	-	0.0003	1	μA



SPECIFICATIONS ($V_+ = 3\text{ V}$)								
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V_+ = 3\text{ V}, \pm 10\%, V_{IN} = 0.4\text{ V or }1.4\text{ V}^e$	TEMP. ^a	LIMITS -40 °C to 85 °C			UNIT	
				MIN. ^b	TYP. ^c	MAX. ^b		
Analog Switch								
Analog signal range ^d	V_{NO}, V_{NC} V_{COM}		Full	0	-	V_+	V	
On-resistance	R_{ON}	$V_+ = 2.7\text{ V},$ $V_{COM} = 0.2\text{ V} / 1.5\text{ V}, I_{NO}, I_{NC} = 10\text{ mA}$	Room Full ^d	- -	1.4 -	2.5 3	Ω	
R_{ON} flatness ^d	R_{ON} flatness	$V_+ = 2.7\text{ V},$ $V_{COM} = 0\text{ V to }V_+, I_{NO}, I_{NC} = 10\text{ mA}$	Room	-	0.6	0.9		
R_{ON} match ^d	ΔR_{ON}		Room	-	-	0.3		
Switch off leakage current ^f	$I_{NO(off)}$ $I_{NC(off)}$	$V_+ = 3.3\text{ V}$ $V_{NO}, V_{NC} = 1\text{ V} / 3\text{ V}, V_{COM} = 3\text{ V} / 1\text{ V}$	Room	-5	-	5	nA	
			Full ^d	-15	-	15		
	Room		-5	-	5			
	Full ^d		-15	-	15			
Channel-on leakage current ^f	$I_{COM(on)}$	$V_+ = 3.3\text{ V},$ $V_{NO}, V_{NC} = V_{COM} = 1\text{ V} / 3\text{ V}$	Room Full ^d	-5 -15	- -	5 15		
Digital Control								
Input high voltage	V_{INH}		Full	1.4	-	-	V	
Input low voltage	V_{INL}		Full	-	-	0.4		
Input capacitance ^d	C_{IN}		Full	-	3	-	pF	
Input current ^f	I_{INL} or I_{INH}	$V_{IN} = 0\text{ V or }V_+$	Full	-1	-	1	μA	
Dynamic Characteristics								
Turn-on time ^d	t_{ON}	V_{NO} or $V_{NC} = 2\text{ V},$ $R_L = 300\ \Omega, C_L = 35\text{ pF}$	Room	-	21	42	ns	
			Full ^d	-	-	47		
Turn-off time ^d	t_{OFF}		Room	-	16	32		
			Full ^d	-	-	35		
Break-before-make time ^d	t_d			Room	1	7	-	
Charge injection ^d	Q_{INJ}		$C_L = 1\text{ nF}, V_{GEN} = 0\text{ V}, R_{GEN} = 0\ \Omega$	Room	-	6	-	pC
Off-isolation ^d	OIRR		$R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$	Room	-	-63	-	dB
Crosstalk ^d	X_{TALK}			Room	-	-63	-	
Bandwidth ^d	BW		Room	-	160	-	MHz	
N_O, N_C off capacitance ^d	$C_{NO(off)}$ $C_{NC(off)}$	$V_{IN} = 0\text{ V or }V_+, f = 1\text{ MHz}$	Room	-	16	-	pF	
			Room	-	52	-		
Power Supply								
Power supply current	I_+	$V_{IN} = 0\text{ V or }V_+$	Full	-	0.00002	1	μA	



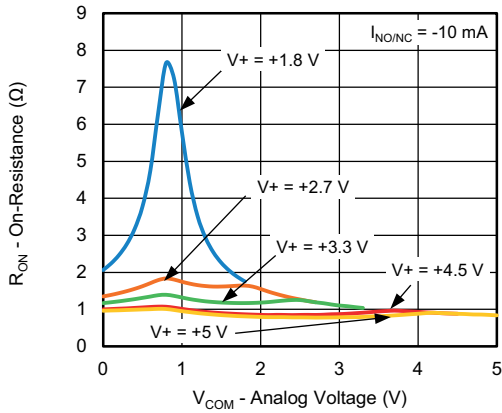
SPECIFICATIONS (V+ = 2 V)								
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 2 V, ± 10 %, VIN = 0.4 V or 1.6 V ^e	TEMP. ^a	LIMITS -40 °C to +85 °C			UNIT	
				MIN. ^b	TYP. ^c	MAX. ^b		
Analog Switch								
Analog signal range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0	-	V+	V	
On-resistance	R _{ON}	V+ = 1.8 V, V _{COM} = 0.2 V / 0.9 V I _{NO} , I _{NC} = 10 mA	Room Full ^d	- -	5 -	10 15	Ω	
R _{ON} flatness ^d	R _{ON} flatness	V+ = 1.8 V, V _{COM} = 0 V to V+, I _{NO} , I _{NC} = 10 mA	Room	-	6	9		
R _{ON} match ^d	ΔR _{ON}		Room	-	-	0.3		
Switch off leakage current ^f	I _{NO(off)} I _{NC(off)}	V+ = 2.2 V V _{NO} , V _{NC} = 0.5 V / 1.5 V, V _{COM} = 1.5 V / 0.5 V	Room	-0.5	-	0.5	nA	
			Full ^d	-5	-	5		
	Room		-0.5	-	0.5			
	Full ^d		-5	-	5			
Channel-on leakage current ^f	I _{COM(on)}	V+ = 2.2 V, V _{NO} , V _{NC} = V _{COM} = 0.5 V / 1.5 V	Room Full ^d	-0.5 -5	- -	0.5 5		
Digital Control								
Input high voltage	V _{INH}		Full	1.6	-	-	V	
Input low voltage	V _{INL}		Full	-	-	0.4		
Input capacitance ^d	C _{IN}		Full	-	3	-	pF	
Input current ^f	I _{INL} or I _{INH}	V _{IN} = 0 V or V+	Full	-1	-	1	μA	
Dynamic Characteristics								
Turn-on time ^d	t _{ON}	V _{NO} or V _{NC} = 1.5 V, R _L = 300 Ω, C _L = 35 pF	Room	-	37	57	ns	
			Full ^d	-	-	60		
Turn-off time ^d	t _{OFF}		Room	-	26	44		
			Full ^d	-	-	45		
Break-before-make time ^d	t _d			Room	1	17		-
Charge injection ^d	Q _{INJ}		C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room	-	21		-
Off-isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room	-	-63	-	dB	
Crosstalk ^d	X _{TALK}		Room	-	-63	-		
N _O , N _C off capacitance ^d	C _{NO(off)} C _{NC(off)}	V _{IN} = 0 V or V+, f = 1 MHz	Room	-	16	-	pF	
			Room	-	51	-		
Channel-on capacitance ^d	C _{ON}		Room	-	51	-		
Power Supply								
Power supply current	I+	V _{IN} = 0 V or V+	Full	-	0.00001	1	μA	

Notes

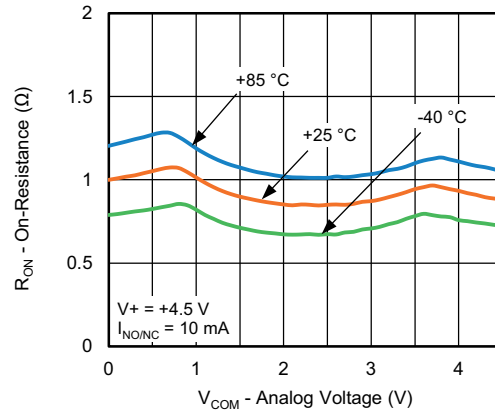
- a. Room = 25 °C, full = as determined by the operating suffix
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
- c. Typical values are for design aid only, not guaranteed nor subject to production testing
- d. Guarantee by design, nor subjected to production test
- e. V_{IN} = input voltage to perform proper function
- f. Guaranteed by 5 V leakage testing, not production tested



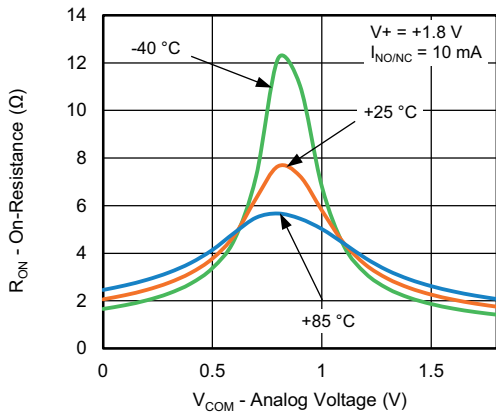
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



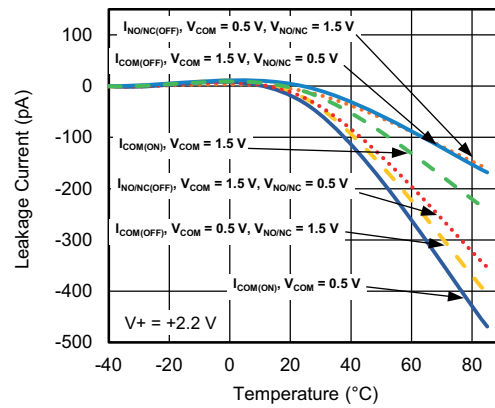
RON vs. VCOM and Supply Voltage



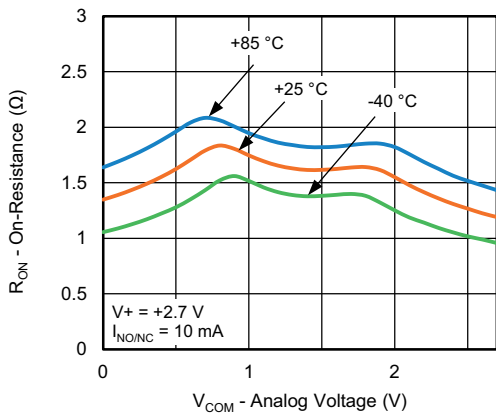
RON vs. VCOM and Temperature



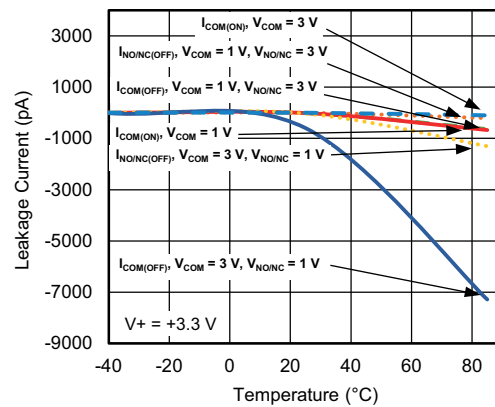
RON vs. VCOM and Temperature



Leakage Current vs. Temperature

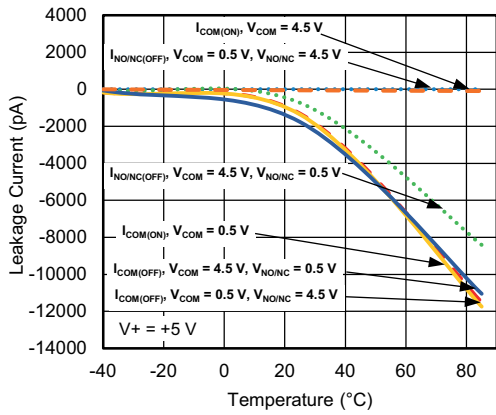


RON vs. VCOM and Temperature

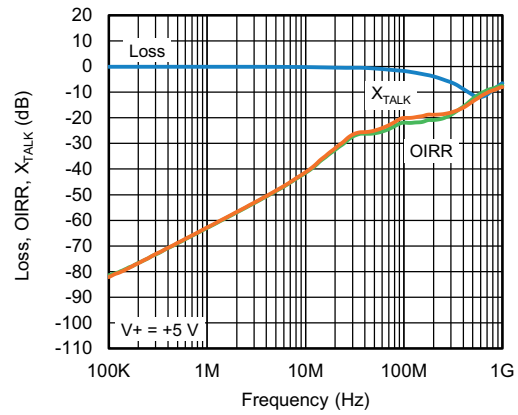


Leakage Current vs. Temperature

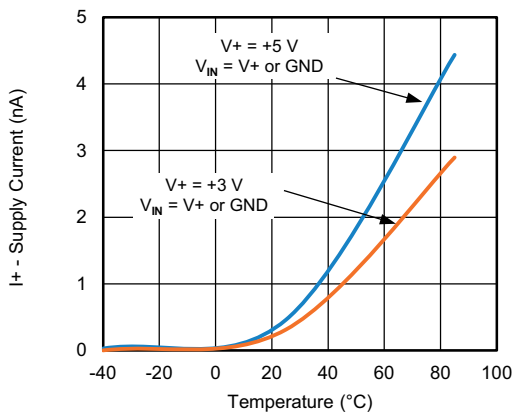
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



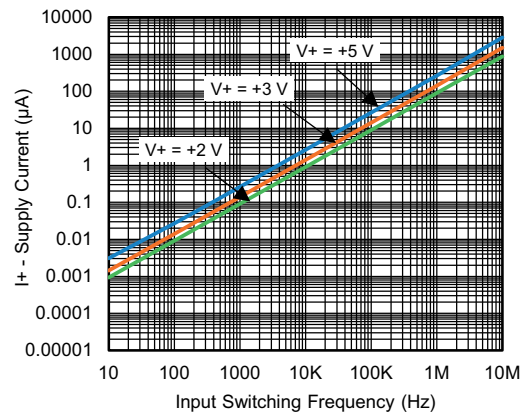
Leakage Current vs. Temperature



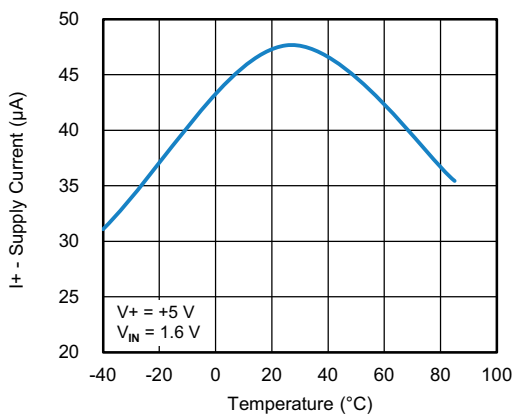
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



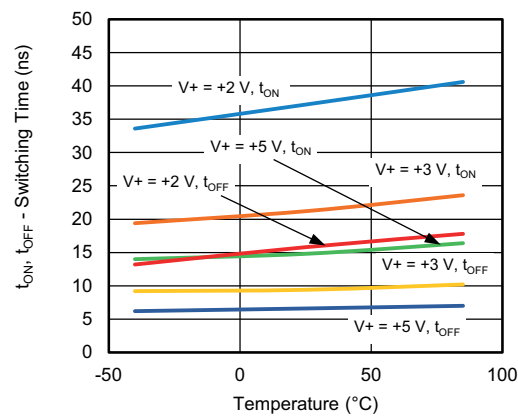
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

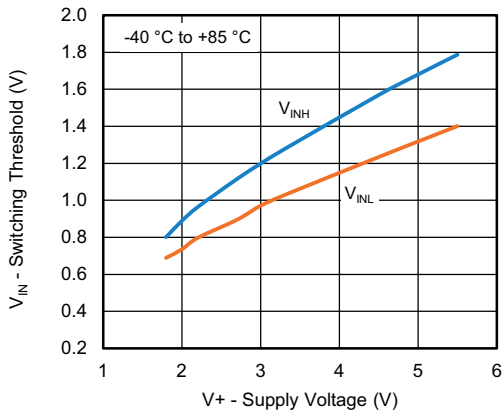


Supply Current vs. Temperature

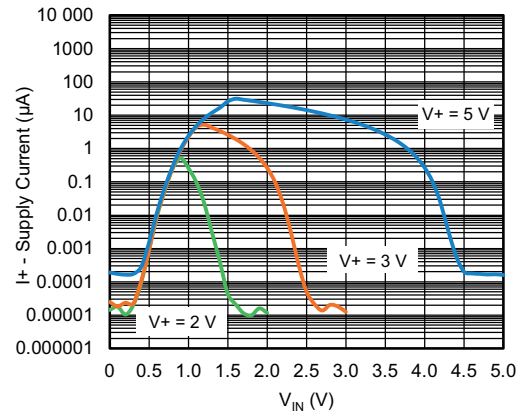


Switching Time vs. Temperature and Supply Voltage

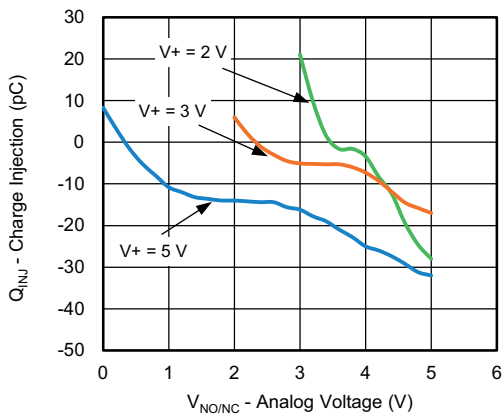
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



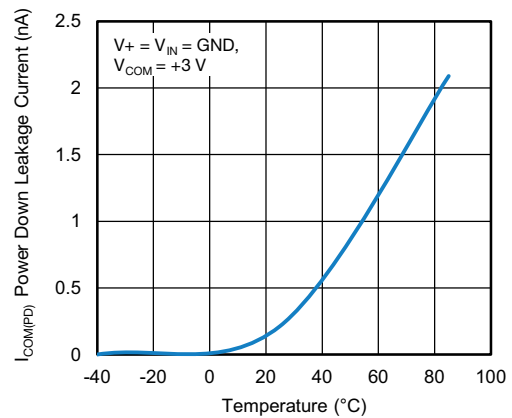
Switching Threshold vs. Supply Voltage



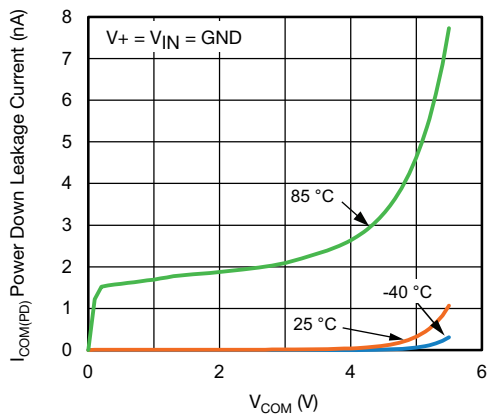
Supply Current vs. Enable Input Voltage



Charge Injection vs. Analog Voltage

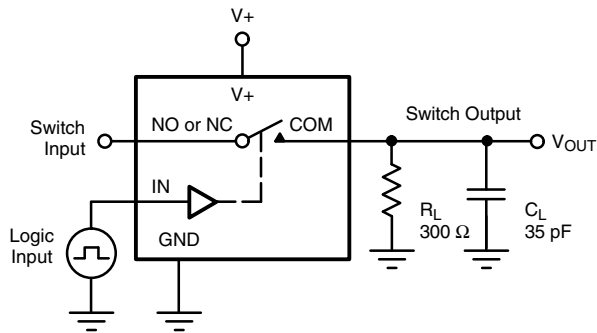


Power Down Leakage Current vs. Temperature



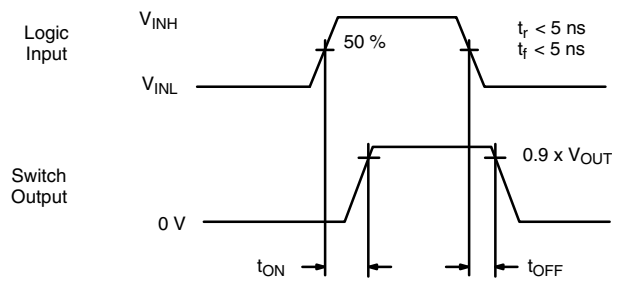
Power Down Leakage Current vs. V_{COM}

TEST CIRCUITS



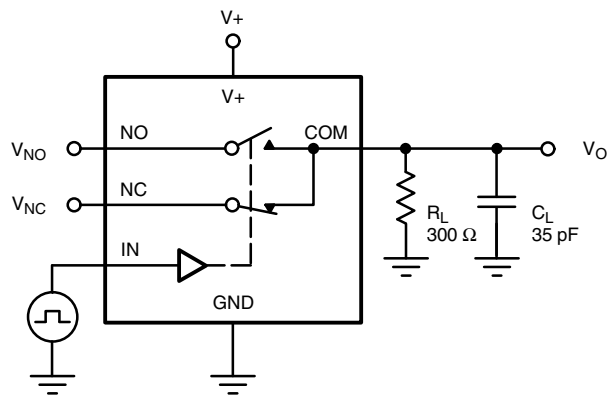
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time



C_L (includes fixture and stray capacitance)

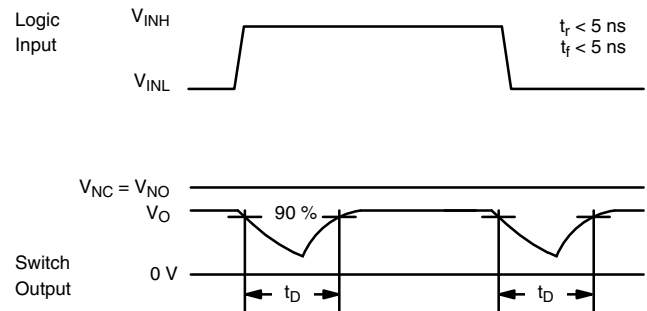
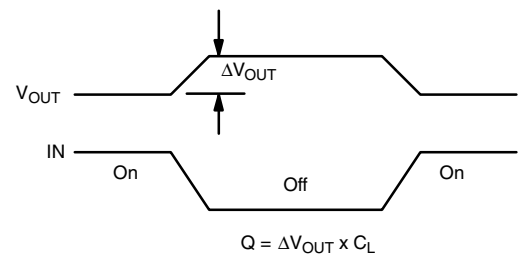
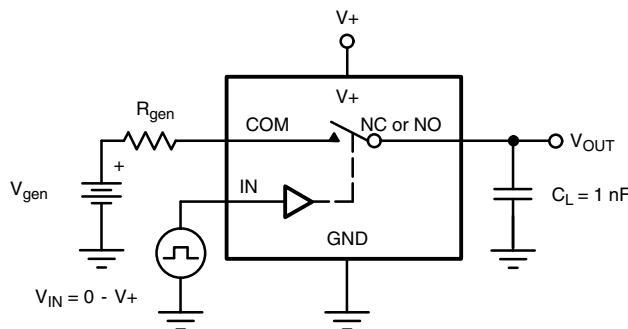
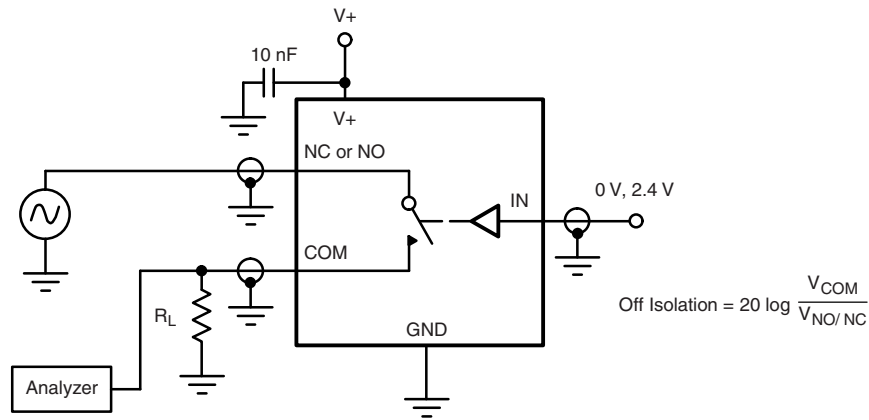
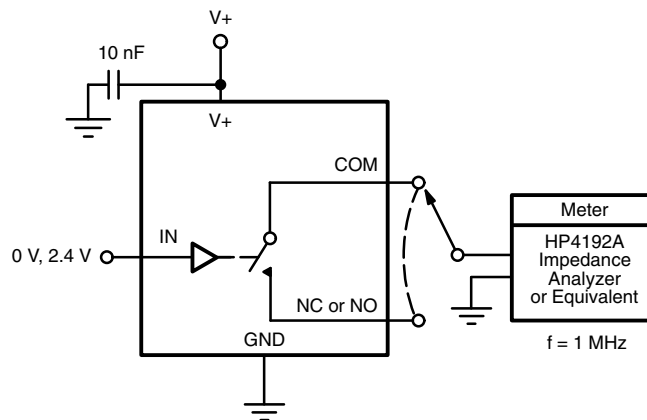


Fig. 2 - Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection

TEST CIRCUITS

Fig. 4 - Off-Isolation

Fig. 5 - Channel Off / On Capacitance

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